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Selective p- and n-Doping of Colloidal PbSe Nanowires To Construct Electronic and Optoelectronic Devices

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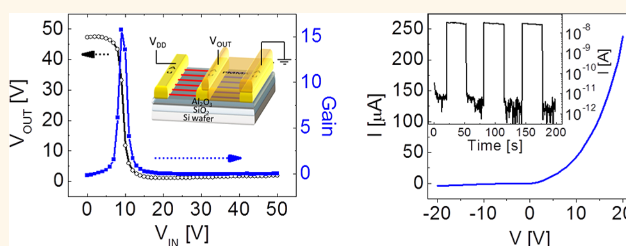
ABSTRACT We report the controlled and selective doping of colloidal PbSe nanowire arrays to define pn junctions for electronic and optoelectronic applications. The nanowires are remotely doped through their surface, p-type by exposure to oxygen and n-type by introducing a stoichiometric imbalance in favor of excess lead. By employing a patternable poly(methyl)methacrylate blocking layer, we define pn junctions in the nanowires along their length. We demonstrate integrated complementary metal-oxide semiconductor inverters in axially doped nanowires that have gains of 15 and a near full signal swing. We also show that these pn junction PbSe nanowire arrays form fast switching photodiodes with photocurrents that can be optimized in a gated-diode structure. Doping of the colloidal nanowires is compatible with device fabrication on flexible plastic substrates, promising a low-cost, solution-based route to high-performance nanowire devices.



KEYWORDS: PbSe · colloidal nanowires · selective doping · pn junction · CMOS inverter · photodiode

Colloidal semiconductor nanostructures are of great interest for their unique size-dependent electronic and optical properties and for their solution-based processability that allows these materials to be integrated and their properties to be exploited in devices.[1−3] Among nanostructures, colloidal PbSe nanowires (NWs) are of particular interest because lead chalcogenides have large exciton, electron, and hole Bohr radii, a narrow and widely size tunable band gap, high and similar electron and hole mobility, and anisotropic properties along their one-dimensional axis.[4,5] They are also explored for their potential for multiexciton generation.[6−8] The unique properties of PbSe nanostructures make them promising semiconductor building blocks in electronic circuitry,[9] multijunction solar cells,[10] near- to mid-infrared photodetectors,[11−13] and high-temperature thermoelectrics.[14,15] Curiously, while bulk PbSe or PbS are the mainstay of near- to mid-infrared photoconductor-based photodetectors, they have not been used to develop photodiodes. The lead chalcogenides lost in the commercial arena to HgCdTe detectors many years ago because of their high thermal mismatch to underlying substrates, which causes mechanical failure upon thermal cycling,[16] and their high dielectric constant, which resulted in long *RC* (product of resistance and capacitance) time constants.[17] These two limitations are no longer relevant in today's imaging technology and are overcome in NWs by the low-temperature and solution-based fabrication of devices. However, there are few reports integrating lead chalcogenide NWs in devices, primarily because of the lack of methods reported to controllably dope these materials.

In this work, we demonstrate processes to selectively p- and n-dope PbSe NW arrays and design pn junctions for electronic and optoelectronic applications. We take advantage of the high surface area of the NWs to remotely dope the NWs by introducing adatoms at their surface. The p-doping is created simply by exposure to oxygen, which introduces acceptors with low ionization

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energy, as we have shown previously.[18,19] The n-doping is realized by applying vacuum- and solution-based methods to produce an excess of lead, which we demonstrated dopes analogous zero-dimensional nanocrystal films[9,20,21] and here show that the stoichiometric imbalance is effective at creating donors in PbSe NWs.

Employing a poly(methyl methacrylate) (PMMA) blocking layer in our process, we selectively p- and n-dope the NWs to define pn junctions along their lengths. We create axial p- and n-type field-effect transistors (FETs) as building blocks to demonstrate integrated colloidal PbSe NW array complementary metal-oxide semiconductor (CMOS) inverters. The NW CMOS inverters show gains of 15 for signal amplification and inversion of logic output at low and high input voltages for signal switching. We also define pn junctions in NW arrays to create photodiodes that switch >1000 faster than NW array photoconductors. By integrating the NW array pn junctions in a gated-diode structure, we control the carrier statistics and the dimensions of the depletion region to enhance charge carrier collection. To the best of our knowledge, this is the first report demonstrating colloidal NW-integrated electronic circuits and also the first example of colloidal pn junction NW optoelectronic devices. We show that our selective doping processes for PbSe NW arrays are compatible with device fabrication on flexible plastics.

RESULTS AND DISCUSSION

We synthesize colloidal PbSe NWs that are 10 nm in diameter and >10 μm in length.[22] Hexadecyl-*graft*-polyvinylpyrrolidone (HD-PVP, 1%) is added to stabilize the NWs in octane. PbSe NW array FETs are fabricated as a platform to investigate NW doping. Heavily n-doped Si wafers with 250 nm of thermally grown SiO_2 are used as substrates and serve as a back gate and a part of the gate dielectric layer of the FET, respectively. Al_2O_3 (20 nm) is deposited by atomic layer deposition to complete the gate dielectric stack and to reduce the dielectric−semiconductor interface trap density and device hysteresis. Source and drain electrodes are patterned *via* standard photolithography and thermal evaporation of Au to define FET channels with a length of 20 μm and a width of 300 μm. Substrates are immersed in a solution of (3-mercaptopropyl)trimethoxysilane (MPTS) (5 vol % in toluene) for 24 h to enhance the NW−substrate adhesion and further reduce the device hysteresis.[23] PbSe NWs are electrophoretically aligned across the channel of the FET by depositing a drop of the NW dispersion in octane onto the gate dielectric surface while applying an electric field of 10^4−10^5 V/cm across the junction.[24] The octane is allowed to evaporate, and then the samples are washed with methanol and chloroform to remove impurities, excess organic compounds, and polymer. The PbSe NW FETs are immersed in a 10 mM solution of NH_4SCN[25−28] in methanol to remove the bulky insulating tetradecylphosphonic acid and oleic acid ligands used in synthesis and displace the HD-PVP used to aid dispersion and replace them with the compact thiocyanate ligand (Supporting Information Figure S1A). Ligand exchange reduces the device contact resistance and enhances the conductivity.[19] TEM images (Supporting Information Figure S1B−D) confirm that ligand exchange with thiocyanate does not change the PbSe NW morphology, in agreement with a previous report,[29] and does not lead to NW agglomeration.

Figure 1A depicts an aligned PbSe NW array FET. As-prepared and thiocyanate-exchanged PbSe NW FETs show ambipolar characteristics seen by v-shaped transfer characteristics (Figure 1B, black curve) and by an increase in current at low V_G and high V_{DS} in the output characteristics (Figure 1C), as electrons (holes) are injected at the drain electrode in the hole (electron) accumulation regimes.[29] Ambipolar behavior in PbSe NW FETs is consistent with the similar electron and hole effective masses and the mirror-like electronic structure of PbSe, as previously reported.[5]

Figure 1A also portrays the general scheme we use to investigate the doping process and create p-type or n-type devices. For this purpose, we introduce surface adatoms to remotely dope the NWs. We expose the NW arrays to controlled doses of oxygen gas in a UV-ozone chamber to produce p-doping. Foreign oxygen atoms are known to create acceptor states in lead chalcogenide nanostructures, thin films, and bulk crystals.[18,19,30−32] To n-dope the PbSe NWs, we introduce excess lead ions or atoms to generate a stoichiometric imbalance through solution-based $PbCl_2$ treatment in oleylamine or through thermal evaporation of elemental lead, respectively. Lead enrichment and therefore chalcogen vacancies are known to create donor states in lead chalcogenides[30] and, as we have shown, in lead chalcogenide nanocrystal thin films.[9,20,21]

The transfer characteristics in Figure 1B show that oxygen and lead adatoms successfully dope the PbSe NWs, transforming the ambipolar, thiocyanate-exchanged FETs into p-type and n-type FETs, respectively. Excess oxygen (lead) enhances the hole (electron) current, reduces the electron (hole) current, and shifts the threshold voltage (V_{TH}) to positive (negative) voltages, reflecting a shift in the Fermi level toward the valence (conduction) band.[20] The hysteresis in the transistor characteristics is dominated by trap states at the semiconductor NW−gate dielectric interface.[23] Optimization of the gate dielectric surface modification and pn junction fabrication process may reduce the device hysteresis and increase the noise margin for electronic circuitry. The output characteristics of the oxygen p-doped and lead n-doped FETs are shown in the respective hole and electron accumulation regimes in Figure 1D. Comparison between the

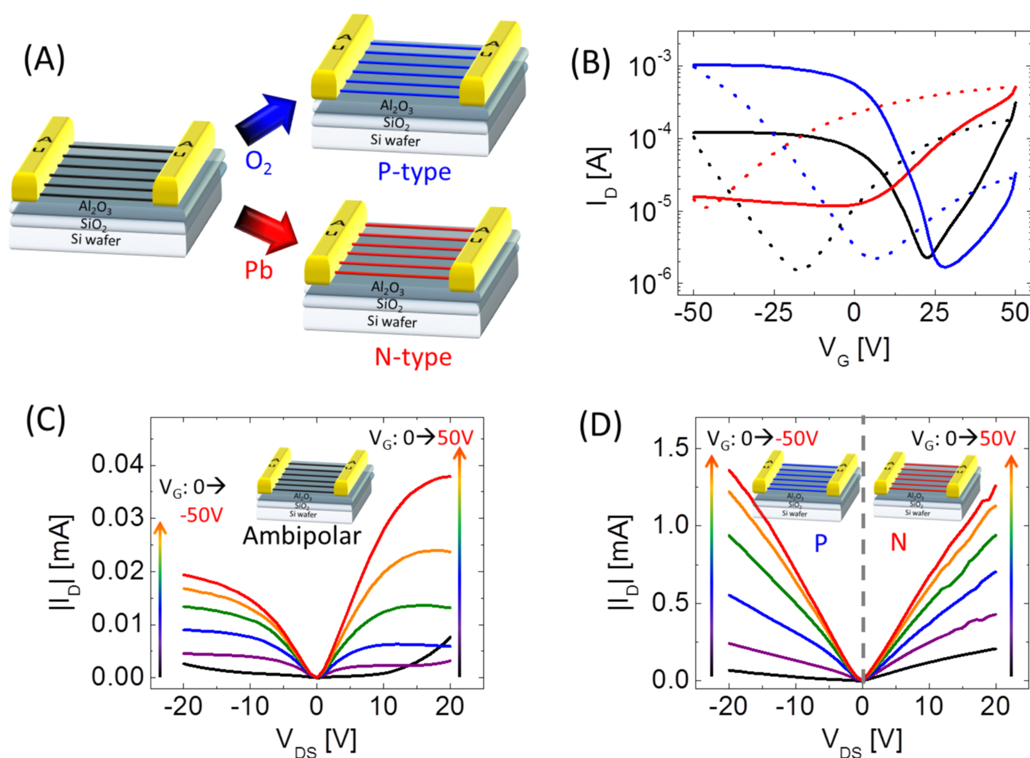

Figure 1. (A) Schematic of PbSe NW FETs and their p-type and n-type doping through the introduction of surface oxygen and excess lead atoms. (B) Transfer characteristics at V_{DS} = ±20 V for PbSe NW FETs before (black) and after oxygen (blue) exposure or lead (red) deposition by thermal evaporation (solid line represents the forward sweep, and dotted line represents the reverse sweep). Output characteristics of (C) undoped PbSe NW FETs and (D) oxygen-doped p-type (left) and lead-doped n-type PbSe NW FETs (right).

output characteristics of ambipolar FETs (Figure 1C) and p-type and n-type FETs (Figure 1D) emphasizes the 50× increased hole and electron currents achieved through doping, as the carrier concentrations are increased and the carrier mobilities are increased due to trap state filling discussed below.

We estimate the effective mobilities of the PbSe NW FETs from the transfer characteristics by using the lithographically patterned channel dimensions (*i.e.*, assuming the channel is completely filled with NWs and that it serves as a thin film). We note here that calculating the mobility using the Wunnicke capacitance[33] for each nanowire gives similar values. The actual coverage of the channel is less than 10%, and therefore, the device mobilities underestimate the PbSe NW carrier mobilities by >10×. The saturation regime electron mobility for n-type NW FETs is 11 ± 2.5 cm^2/Vs, and the hole mobility for p-type NW FETs is 15 ± 2 cm^2/Vs, both of which are higher than those of ambipolar NW FETs (electron mobility = 0.8 ± 0.2 cm^2/Vs and hole mobility = 1.3 ± 0.3 cm^2/Vs). Similar mobilities are found from the linear regime characteristics, with an electron mobility of 10 ± 1.4 cm^2/Vs for n-type FETs, a hole mobility of 15 ± 2.2 cm^2/Vs for p-type FETs, and electron and hole mobilities of 0.7 ± 0.2 and 1.2 ± 3 cm^2/Vs for ambipolar FETs, respectively. The increase in mobility upon n- or p-doping is attributed to the filling of trap states introduced by unsatisfied bonding at the NW surface and by the NW–gate dielectric interface.[20,34] After doping, the I_{ON}/I_{OFF} of the NW FET ratio increases from ~100 to ~1000, as I_{ON} increases more significantly than the increase in I_{OFF}. This is consistent with the transport of a greater concentration of carriers with high mobility in the on-state, as traps are filled and carriers occupy higher energy states, in comparison to the carrier transport in the off-state.

The p- and n-doping of the PbSe NW arrays can be controlled by the "dose" of the treatment used to introduce oxygen or excess lead. By increasing the exposure time of the FET in the UV-ozone, the oxygen p-doping increases and the FET behavior is modulated from ambipolar to lightly p-type and eventually to heavily p-type (Supporting Information Figure S2A). By increasing the time that the device is placed in the $PbCl_2$ solution in oleylamine, a greater number of lead ions are bound to the NW surface and the device becomes more n-doped (Supporting Information Figure S2B,C). In the case of the thermal evaporation method, the more lead deposited, the more n-type the FETs become. If too much lead (>12 Å) is evaporated, the device becomes heavily doped and shows semimetallic, degenerate behavior (Supporting Information Figure S2D).

We estimate the change in electron (Δn) or hole (Δp) concentration with the dose of the treatment used to dope the NWs by Δn or $\Delta p = \Delta V_{TH} C_{ox}/q$, where ΔV_{TH} is

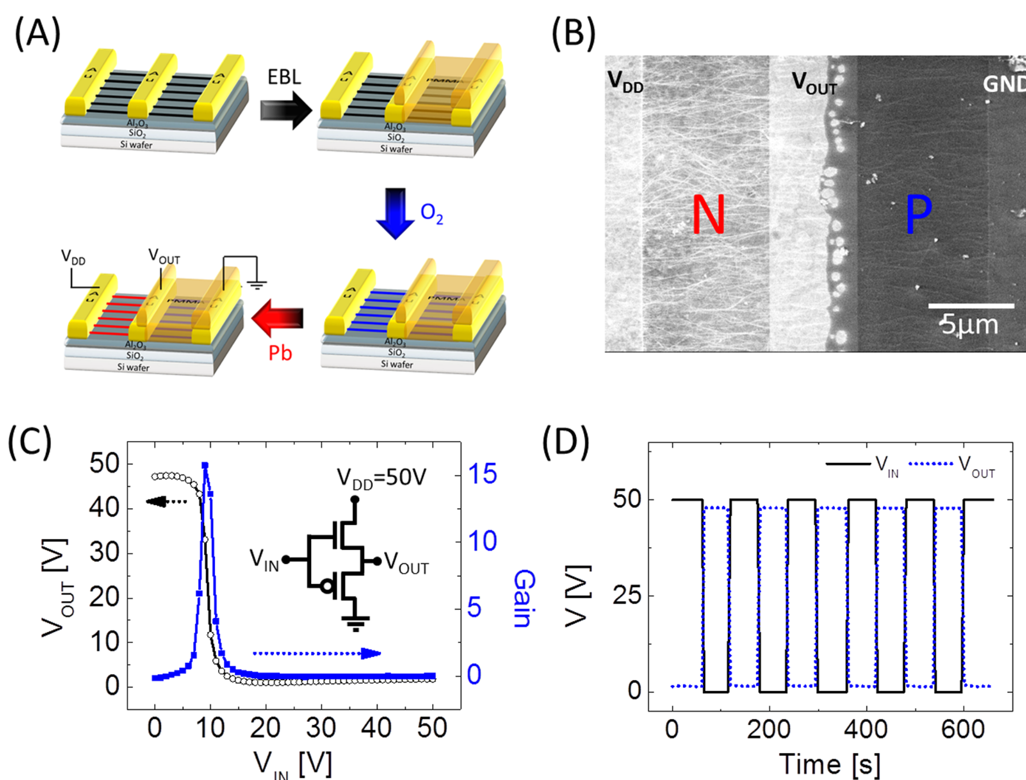

Figure 2. (A) Schematic of the fabrication process and (B) SEM image of an integrated CMOS PbSe NW array inverter created by p-doping through exposure to oxygen and n-doping through thermal evaporation of lead. (C) Voltage transfer characteristics and (D) switching behavior of the inverter in response to a square wave input. Inset in (C) is the circuit diagram of the CMOS inverter.

the shift in the threshold voltage extracted from the transfer characteristics,[35−38] C_{ox} is the capacitance of the oxide layer (1.33 nF/cm^2), and q is electrical charge. For example, a ΔV_{TH} of -10 V is seen in NW FETs by thermal evaporation of 4 Å of lead or by immersion in a $PbCl_2$ solution at 80 °C for 10 min, resulting in an increase in mobile electron density of $\sim 7 \times 10^{17}$/cm^3. A ΔV_{TH} of $+10$ V is realized by a 1 min exposure of the NWs to oxygen, now increasing the hole density by $\sim 7 \times 10^{17}$/cm^3. These doping levels are similar to those we reported previously for the introduction of excess lead in nanocrystal thin films.[20,21]

Utilizing these doping methods, we fabricate pn junctions in the PbSe NWs of the arrays to build integrated CMOS inverters. For the example of the CMOS inverter, we begin by using electron-beam lithography and thermal evaporation of Au to pattern three electrodes in parallel. We deposit aligned NWs across the device by applying the electric field between the outer pair of electrodes. The distance between the outer pair of electrodes is 20 μm, as we used above, and the added middle electrode is 4 μm, defining left and right FETs with channel lengths of 8 μm. To selectively dope one side of the junction, the other side needs to be protected from doping. We use PMMA as an electron-beam-sensitive, patternable blocking layer. We found that while the PMMA is permeable to oxygen and therefore does not serve as a blocking layer toward oxygen, PMMA is a suitable blocking layer for the solution-based addition or thermal evaporation of excess lead, protecting the PbSe NWs underneath from n-doping (Supporting Information Figure S3). To define pn junctions in the NWs, we start by coating the NW arrays with PMMA and then use electron-beam lithography to pattern the PMMA blocking layer on top of the NWs. We p-dope the entire length of the NWs with oxygen and finally selectively n-dope the exposed side of the NWs in the arrays with excess lead. The patterning of the PMMA blocking layer by electron-beam lithography is aligned with the underlying electrodes to fabricate adjacent p-type and n-type FETs that share in common the middle electrode. This acts to tie the drain electrodes of the n-type and p-type FETs, constructing the integrated CMOS inverter (Figure 2A). Figure 2B shows an SEM image of a completed PbSe NW array CMOS inverter. We confirm that the FET on the right shows p-type characteristics and that on the left shows n-type characteristics (Supporting Information Figure S4).

The electrical characteristics of the NW CMOS inverter are measured using four probes: three contacts to the electrodes and one to the back gate. The n-type FET has its source electrode connected to the inverter's supply voltage (V_{DD}). The common electrode that serves as the drain terminals of the n-type FET and p-type FET is connected to the inverter's output (V_{OUT}). The source electrode of the p-type FET is connected to ground (V_{SS}).

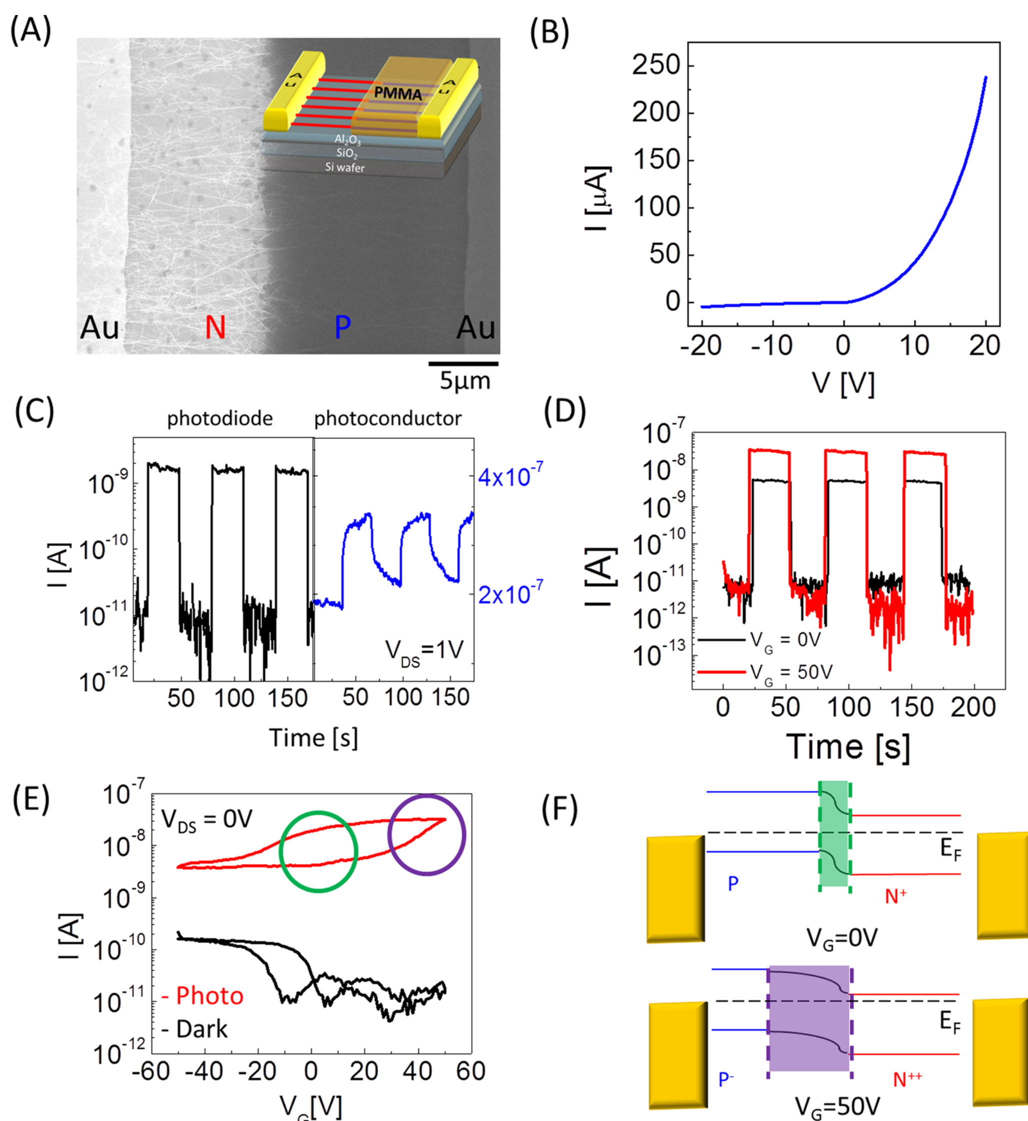

Figure 3. (A) SEM image and (inset) schematic of a PbSe NW array pn junction diode fabricated by p-doping through exposure to oxygen and n-doping through thermal evaporation of lead. (B) Dark current–voltage characteristics of the PbSe NW array pn junction diode. (C) Dynamic response of (left) the NW array pn junction photodiode in comparison to that for (right) a NW array p-type photoconductor. (D) Dynamic response (black) at V_G = 0 V and (red) V_G = 50 V and (E) transfer characteristics at V_{DS} = 0 V (black) before and (red) upon illumination of a gated PbSe NW array pn junction. The photoresponse in (C–E) is probed using ~1.2 mW/cm^2 488 nm excitation. (F) Schematic of the energy band diagram of the gated PbSe NW photodiode (top) at V_G = 0 V and (bottom) at V_G = 50 V.

The common back gate of the FETs is connected to the inverter's input (V_{IN}). Figure 2C (black curve) shows the voltage transfer characteristics of the fabricated NW CMOS inverter. At V_{IN} = 10 V, the inverter operates as an amplifier with a gain (dV_{OUT}/dV_{IN}) of approximately 15 (blue curve). At V_{IN} < 5 V or V_{IN} > 15 V, the inverter operates as a switch, inverting low V_{IN} to high V_{OUT} and high V_{IN} to low V_{OUT}.

Figure 2D shows the dynamic response of the NW CMOS inverter at V_{DD} = 50 V to a square wave input signal V_{IN} that switches from 0 to 50 V with a 200 s period and a 50% duty cycle. The output voltage V_{OUT} is a NOT logic function to the input signal V_{IN}. The values of V_{OUT} are measured to be ~48 and ~0.9 V for V_{IN} at 0 and 50 V, respectively, utilizing ~94% of the 50 V supply voltage. The nearly ideal switching behavior demonstrates the PbSe NW CMOS inverter function and its potential in electronic applications.

We further examine the possibility of adopting this technology to demonstrate optoelectronic devices. Using the processes described above, we fabricate PbSe NW array-gated pn junction diodes (Figure 3A). One signature of successful PbSe NW array pn junction formation is the rectifying behavior of the diode, seen in the dark current–voltage characteristics of the device (Figure 3B). The n-doping of the pn junction diodes may be carried out either through the solution-based $PbCl_2$ method or through thermal evaporation of elemental lead (Supporting Information Figure S5). The diode shows a rectification ratio of forward/reverse current

of ~60. While the pn junction shows rectifying behavior, the ideality factor is somewhat large at ~10 as we have not engineered the metal–semiconductor junction to form low resistance contacts and we expect partial Fermi level pinning.[18] Assuming an intrinsic carrier concentration of $n_i = 4 \times 10^{14}/cm^3$ from the ~0.45 eV band gap of the NWs[18,19] and acceptor (N_A) and donor (N_D) doping concentrations of $7 \times 10^{17}/cm^3$ (extracted from ΔV_{TH} above) by 1 min exposure to oxygen for p-doping and by deposition of ~4 Å of lead for n-doping, we calculate a built-in potential

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) = \sim 0.38 \text{ eV}$$

and a depletion width[36]

$$W = \sqrt{\frac{2\varepsilon_s \varepsilon_0}{q}\left(\frac{N_D + N_A}{N_D N_A}\right) V_{bi}} = \sim 200 \text{ nm}$$

Here k_B is Boltzmann's constant, T is temperature, ε_s is the permittivity of ~200 for PbSe, and q is electrical charge.

We probe the switching response of the pn junction diode photocurrent to pulsed photoexcitation (Figure 3C, left). Photocurrent is generated upon illumination at $V_{DS} = 0$ V, reflecting the formation of a pn junction and a built-in potential. No current is detected in the dark at $V_{DS} = 0$ V, as it falls below the ~10 pA noise level of the instrument. The rise and fall times of our pn junction photodiode are less than the 1 s time resolution shown in Figure 3C (left) and are shorter than 10 ms time resolution of our instruments (Supporting Information Figure S6). For comparison, we fabricate a p-type PbSe NW array photoconductor by doping the whole length of the NWs with oxygen. The NW photoconductor has a switching time greater than a few seconds (Figure 3C, right). We emphasize that the photoresponse of our axially doped pn junction photodiode is >1000 times faster than that of a p-type photoconductor.[36] The responsivity of our photodiode is 0.14 A/W, which is comparable to that for the highest responsivity nanoscale semiconductor photodiodes,[39] which we expect may be increased by optimizing our device.

We further examine the properties of the NW array pn junctions in the dark and under illumination by gating the diodes in the FET platform. By applying a positive gate bias of $V_G = 50$ V, the photocurrent at $V_{DS} = 0$ V is enhanced by an order of magnitude compared to the device operated at $V_G = 0$ V (Figure 3D). The increased photocurrent under the applied gate bias can be understood by comparing measurements of the FET transfer characteristics in the dark and under illumination, as shown in Figure 3E. As the gate bias is swept from negative to positive voltages, a current level is observed at positive voltage that is higher under illumination than in the dark.

A schematic of the gate dependence of the energy band diagram of the pn junction (Figure 3F) depicts the underlying physics. Depending on the amount of oxygen or lead introduced, the degree of p-doping and n-doping on either side of the junction can be controlled. For example, if we introduce more lead, we form a pn$^+$ diode, with a slightly greater majority carrier electron concentration on the n-side than the majority carrier hole concentration on the p-side of the junction. The asymmetric doping of the junction causes the depletion region to extend mostly into the more lightly p-doped side of the junction. The short depletion region limits the collection of photogenerated carriers and therefore the total photocurrent (highlighted by the green circle in Figure 3E and depicted in the corresponding band diagram on the top of Figure 3F). However, under the applied gate voltage, we can tune the carrier concentrations on either side of the junction and therefore tailor the width of the depletion region. As we apply an increasingly positive gate bias, the electron concentration on the n-side of the junction is accumulated and the hole concentration on the p-side of the junction is further depleted. The positive gate bias transforms the as-fabricated pn$^+$ junction into a p$^-$n^{++} junction. Since the width of the depletion region on the p-side increases more than the decrease in the depletion width on the n-side for the same gate bias, the total depletion width is extended and ultimately enhances the photocurrent (highlighted by the purple circle in Figure 3E and depicted in the corresponding band diagram on the bottom of Figure 3F).

For example, a shorter 30 s exposure to oxygen shifts the threshold voltage less than 10 V, creating a hole concentration on the p-side of ~$5 \times 10^{17}/cm^3$, and 10 Å of deposited lead shifts the threshold voltage more than −50 V, creating an electron concentration on the n-side of ~$5 \times 10^{18}/cm^3$. For these doping levels, a junction depletion width of ~150 nm is formed. For the gated-diode structure, we can calculate the change in carrier density $\Delta n = -\Delta p = (\varepsilon_0 \varepsilon_s E)/q$ induced electrostatically by the gate voltage ($V_G = Ed$), where E is the electric field, d is the thickness, and ε_s is the relative permittivity of the dielectric stack.[36] If a positive gate bias of 50 V is applied to electrostatically modulate the carrier concentration through the 250 nm SiO_2 and 20 nm Al_2O_3 gate dielectric stack, the electron concentration increases and the hole concentration decreases by $4.6 \times 10^{17}/cm^3$, assuming 10% coverage of NWs in the thin film. With the applied gate bias, the electron concentration on the n-side would be ~$5.5 \times 10^{18}/cm^3$ and the hole concentration on the p-side would be ~$4 \times 10^{16}/cm^3$. The 2 orders of magnitude drop in the hole concentration on the p-side of the junction would act to increase the depletion width to ~450 nm. The gated-diode structure allows us to electrostatically tune the carrier concentration and thereby optimize the NW pn junction photodiode performance.

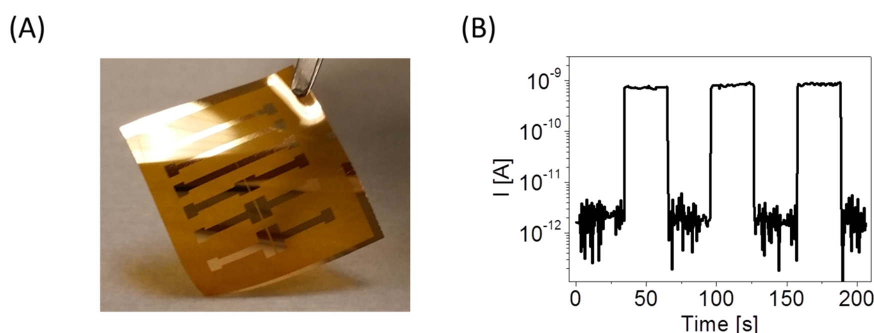

Figure 4. (A) Image of a PbSe NW array photodetector on a flexible Kapton substrate fabricated by p-doping through exposure to oxygen and n-doping through $PbCl_2$ treatment. (B) Dynamic response of a PbSe NW photodetector. The photoresponse in (B) is probed using ~1.2 mW/cm^2 488 nm excitation.

We translate the assembly and selective doping used to fabricate PbSe NW array optoelectronic devices, described above on rigid silicon substrates, to flexible Kapton substrates. Figure 4A shows a photograph of a flexible PbSe NW array photodiode. We show that n-doping the NWs by both solution-based $PbCl_2$ treatment and thermal evaporation of elemental lead is compatible with pn junction fabrication on flexible plastics (Supporting Information Figure S5). The modulation between photocurrent and dark current is still approximately 400−600, comparable to that for the PbSe NW array photodiodes fabricated on rigid substrates (Figure 4B). While we use PMMA as a blocking layer to demonstrate the selective doping and construction of PbSe NW pn junctions, it has limited transmission beyond 2200 nm. For near- or mid-IR detectors, (1) the PMMA could be replaced by optically transparent photo- or e-beam resists, or (2) transparent dielectric materials (*e.g.*, SiO_2, MgF_2) could be deposited and the PMMA lifted off, and then the patterned dielectric material could be used as the blocking layer in the NW pn junction fabrication.

CONCLUSIONS

In conclusion, we demonstrate the selective n- and p-doping of colloidal PbSe NW arrays and exploit axial doping to create pn junction, PbSe NW arrays as the building blocks of integrated electronic circuitry and photodiode-based photodetectors. Scaling to shorter channel lengths and to single NW channel widths promises to optimize device performance for low-voltage, high-speed, and high-density circuits. Higher-performance photodiodes may be realized by scaling the channel length to reduce carrier diffusion through the quasi-neutral regions and by extending these methods for selective doping to construct PIN (p-type/intrinsic/n-type) junctions.

EXPERIMENTAL SECTION

Materials. All manipulations were carried out using standard Schlenk line techniques under dry nitrogen. Tri-*n*-octylphosphine (further referred to as TOP, 90%), oleylamine (70%), oleic acid (OA, 90%), diphenyl ether (99%), lead chloride ($PbCl_2$, 99%), amorphous selenium pellets (99.999%), MPTS (95%), anhydrous methanol, anhydrous isopropyl alcohol, anhydrous acetonitrile, anhydrous hexane, anhydrous chloroform, and anhydrous toluene were bought from Aldrich. Lead acetate trihydrate was purchased from Fisher Scientific Co., and *n*-tetradecylphosphonic acid (TDPA, 97%) was purchased from Strem.

Methods. *PbSe NW Synthesis.* Colloidal PbSe NWs are synthesized by a solution-based chemical method as previously reported.[19,22] First, 0.76 g of lead acetate trihydrate iss dissolved in 2 mL of oleic acid with 10 mL of diphenyl ether. This solution is heated at 150 °C for 30 min under a nitrogen flow to form a lead oleate complex. Subsequently, the solution is allowed to sit and cool to 60 °C. Four milliliters of 0.167 M trioctylphosphine selenide (TOPSe) is added gradually to the existing solution to prevent premature nucleation of PbSe nanostructures. This lead oleate/TOPSe solution is then quickly injected into a prepared solution of 0.2 g of TDPA dissolved in 15 mL of diphenyl ether at 250 °C. The temperature control during this injection step and the subsequent growth step is crucial to the formation of PbSe NWs with a straight morphology. After approximately 50 s of heating and fast stirring, the reaction mixture is cooled to room temperature by using a water bath. The resulting crude solution is then diluted with an equal amount of hexane and then centrifuged at 4000 rpm for 5 min. The precipitated NWs are redispersed in chloroform. Straight NWs with diameters of approximately 10 nm and lengths of >10 μm are formed.

PbSe NW Array FET Preparation. FETs are fabricated on n-doped silicon wafers with 250 nm of thermally grown SiO_2 (Silicon Inc.). Al_2O_3 (20 nm) is deposited as a part of the dielectric stack using atomic layer deposition. The added Al_2O_3 further decreases the FET hysteresis. Photolithography and thermal evaporation of Au are used to define metal electrodes. Devices are thoroughly cleaned with isopropyl alcohol, acetone, and deionized water and by exposure to UV-ozone for 20 min. Devices are then placed in a 5% solution of MPTS in toluene overnight.[21]

The NW dispersion is further diluted in octane to a concentration of 100 g/mL, and several drops of a 10 wt % solution of HD-PVP copolymer in octane are added. The NWs are aligned by the electrophoresis method. The NW dispersion is drop-cast onto the FET channel while applying a dc electric field of 10^4−10^5 V/cm for 10−20 s. The device channel dimensions are 20 μm in length and 300 μm in width. The devices are then washed with methanol and chloroform to remove impurities, excess organic compounds, and polymer. The samples are then immersed in a 10 mg/mL NH_4SCN solution in methanol for 30 s and then thoroughly rinsed with methanol and chloroform to remove excess ligand.

PbSe NW Array pn Junction Preparation. After ligand exchange with thiocyanate, PMMA (from Microchem) 495A4 and

950A4 electron-beam lithography resists are spin-cast at 3000 rpm for 1 min and baked at 180 °C for 3 min sequentially. Electron-beam lithography is used to open a window in the PMMA for selective doping of the exposed side of the NW arrays. After e-beam lithography and development, the device is then annealed at 180 °C for several seconds to get rid of some of the unwanted surface-bound oxygen that is introduced during electron-beam lithography in order to make the NW FETs ambipolar as a starting point. Then, the device is exposed to oxygen for approximately 1 min to p-dope the NWs. Excess Pb, approximately 4 Å, is then thermally evaporated onto the device to n-dope the exposed NWs in the window. It should be noted that $PbCl_2$ treatment can substitute for thermal evaporation to n-dope the NWs. To perform the $PbCl_2$ treatment, the device is immersed in a 10 mM $PbCl_2$ solution in oleylamine for 10 min at 80 °C and washed with hexanes several times.[21] Subsequently, additional PMMA layers are again spin-cast onto the device to minimize NW oxidation.

PbSe NW Array CMOS Inverter. The PbSe NW array CMOS inverter device is prepared following the method used for the PbSe NW array pn junction fabrication, with the addition of a third electrode as a bottom contact. A 4 μm wide third electrode is introduced precisely at the center of the 20 μm gap between the outer electrodes and therefore creates two 8 μm channel length FETs, one that is p-type and the other is n-type.

Characterization. The devices are measured using an Agilent 4156C semiconductor parameter analyzer in combination with the Karl Suss PM5 probe station mounted in the nitrogen environment of a glovebox. Photoconductivity measurements are carried out by introducing 488 nm light from a Coherent Ar:Kr laser through a fiber-optic feedthrough into the glovebox. Photocurrents and dark currents are recorded by using an Agilent 4156C semiconductor parameter analyzer and a mechanical shutter.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: FTIR spectra of PbSe NWs before and after ligand exchange, output characteristics, and transfer characteristics of p-type and n-type PbSe NW FETs and their behavior with blocking layer, pn diode behavior of PbSe NW arrays on flexible substrates, and dynamic response of a gated PbSe NW array pn junction photodiode. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b02734.

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